independent form. Applicants have not, at this juncture, elected to rewrite these claims in independent form and thus submit that these claims remain objected to but allowable.

The rejection of claims 1 and 17 appears to be maintained from the previous Office Action mailed January 13, 2003 in the captioned application. Applicants believe that the arguments presented in the Response to that Office Action (filed March 4, 2003 and received in the PTO on March 11, 2003, referred to as the "Previous Response" below) remain valid. Applicants incorporate the arguments from the Previous Response herein by reference to preserve them for appeal. Applicants respond to the Response to Arguments section of the present Office Action below.

Claim 1 recites a combination of features including: "a segment register configured to store a segment selector identifying a segment descriptor including a first operating mode indication, a second operating mode indication, and one or more bits identifying a segment described by said segment descriptor as a code segment; a control register configured to store an enable indication, wherein said processor is configured to establish a default address size responsive to said enable indication, said first operating mode indication, and said second operating mode indication". In the Response to Arguments Section, the Office Action alleges that the first operating mode indication is the Turley's privilege level (DPL) and that the second operating mode indication is Turley's granularity bit (G). (See Office Action, page 4, item 9). Applicants respectfully disagree.

With regard to the privilege level (DPL), Applicants respectfully submit that Turley has no teaching or suggestion that the DPL is in any way related to default address size. Turley teaches: "This 2-bit field indicates the level of privilege associated with the memory space that the descriptor defines. DPL 0 is most privileged, and DPL 3 the least" (Turley, page 51, paragraph 5). Additionally, Turley teaches the following with regard to privilege level: "Working closely with memory management is a relatively new system of privileged checking...with this method, every piece of code and data is assigned one of four privilege levels, and the processor automatically performs privilege

validation on every memory cycle. If the application is privileged enough, its memory access will be granted. If not, the processor will deny access and generate a privilege fault; the operating system will then take over." (Turley, page 10, last paragraph continuing on to page 11). Thus, the privilege level may be used in determining if a memory access is granted or denied. Applicants respectfully submit that there is no teaching or suggestion in Turley that the privilege level is a first operating mode indication "wherein said processor is configured to *establish a default address size* responsive to said enable indication, *said first operating mode indication*, and said second operating mode indication".

Furthermore, Turley teaches the following regarding the granularity (G) bit: "When this bit is cleared, the 20-bit limit field is assumed to be measured in units of 1 byte. If it is set, the limit field is in units of 4096 bytes" (Turley, page 52, third paragraph). Turley further teaches: "The granularity bit allows you to build a segment larger than 1 MB." (Turley, page 54, second paragraph). Thus, the granularity bit, in conjunction with the limit field, defines the size of a segment. This does not teach or suggest a second operating mode indication "wherein said processor is configured to *establish a default address size* responsive to said enable indication, said first operating mode indication, and *said second operating mode indication*".

The last sentence of item 9 in the Office Action states that "Applicants admit in their argument that there is an enable indication for the default address size". Applicants respectfully disagree with the alleged admission. Nothing in Applicants' remarks is an admission as alleged in the Office Action. Applicants arguments highlight some features of certain claims as an example of why such claims are patentable over the applied references (see, e.g., the second sentence under the heading "Turley, and Turley in view of Khalidi" on page 4 of the Previous Response). Additionally, Applicants conclude that claim 1 is patentable for at least the arguments provided in the Response (see page 6 of the Previous Response, third paragraph). Nothing in Applicants arguments should be taken as an admission. Furthermore, Applicants note that the enable indication is included in the portion of claim 1 quoted in the argument.

Finally, Applicants note the Office Action's statement that the rejection over Hammond in view of Intel is withdrawn due to claim amendments. Applicants submit that the claim amendments were not needed to overcome Hammond in view of Intel since Hammond in view of Intel did not form a *prima facie* case of obviousness of the claims, as detailed in the Previous Response.

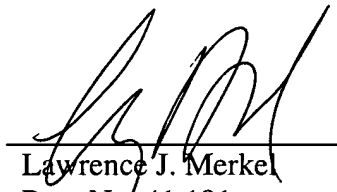
CONCLUSION

Applicants submit that the application is in condition for allowance, and an early notice to that effect is requested. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-54700/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



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Date: 5/29/03